

### REMARKS/ARGUMENTS

Claim 1 is unchanged. Claims 2-17 have been added.

It is noted that the specification filed in this case is in the form of the substitute specification that was filed on February 18, 2004 in the parent application (No. 10/262,567). That substitute specification was accepted by the Examiner in the parent case.

The amendments to the specification made herein are intended to conform the specification to the amendments in the drawings, described in the preceding section, and to correct several remaining clerical and syntactical errors. No new matter has been added.

A complete set of formal drawings is submitted herewith.

Should the Examiner have any questions about any of the amendments made herein, the Examiner is invited to call the undersigned at (408) 982-8201.


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Attorney for Applicant(s)

8/8/05  
Date of Signature

Respectfully submitted,

  
David E. Steuber  
Attorney for Applicant(s)  
Reg. No. 25,557

**Amendments to the Drawings:**

The enclosed Submission of Formal Drawings includes changes to Figs. 14A-14E, 14H-14P, 15A, 16A, 16B, 16D, 16F, 17P-17CC (now Figs. 17O-17BB), 18B (now Fig. 18B-4), 18C, 18H, 19H, 33D and 64B.

The following is an itemization of the changes:

In Figs. 14A-14E, 14H-14P, 15A, 16A, 16B, 16D and 16F, in a number of instances the reference numeral PW5 has been changed to PW5B, the reference numeral NW5 has been changed to NW5B, the reference numeral PW12 has been changed to PW12B, and the reference numeral NW12 has been changed to NW12B, as shown on the enclosed Annotated Sheets. These changes are clearly supported, for example, at page 36, lines 14-17, of the substitute specification filed February 18, 2004, where it is indicated that the suffix "B" is used to denote an implanted layer of dopant as opposed to a "well" of dopant. In any event, these changes are merely changes in labeling and as such do not constitute new matter.

Figs. 17P-17CC have been renumbered as Figs. 17O-17BB, respectively, to rectify the omission of Fig. 17O from the application as filed.

To make the drawings more legible, Figs. 18A and 18B have each been split into four drawings, designated Figs. 18A-1 to 18A-4 and Figs. 18B-1 to 18B-4, respectively. The subject matter in Figs. 18A-1 to 18A-4 and 18B-1 to 18B-3 is unchanged. In Fig. 18B-4, the reference numeral 354M has been replaced by the numeral 354L. The numeral 354M was an error. There is no such reference numeral in the application as filed.

In Fig. 18C, the reference numeral 364P, which is referred to at page 66, line 4, of the substitute specification, has been added, and the designation of the source-body contact has been corrected from "S/D" to "S/B".

In Fig. 18H, reference numeral applicable to the well NW5 has been changed from 354R to 354S to eliminate the conflict with the similarly numbered element in Fig. 18G; and

the reference numeral applicable to the deep N layer has been changed from 390G to 390H to eliminate the conflict with the similarly numbered element in Fig. 35A.

In Fig. 19H, the reference numeral 387 has been corrected to 320 to correspond to the designation of the DMOS transistor at page 70, line 7, of the substitute specification.

In Fig. 33D, the reference numeral 486 has been deleted. It is not referenced in the substitute specification.

In Fig. 64B, the description of the 5 volt transistor 306 as been corrected to "PNP."

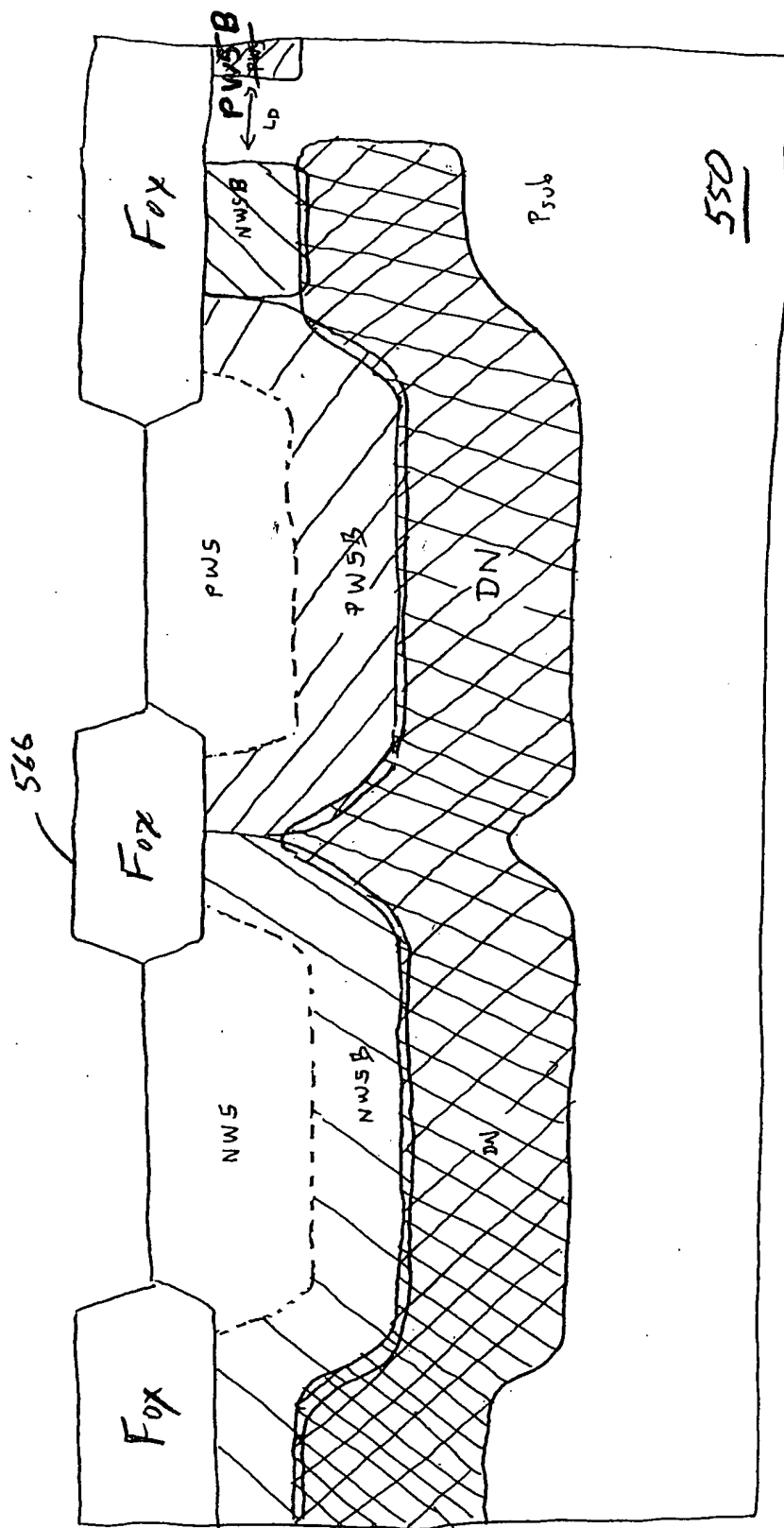
All of the foregoing changes are shown in red in the enclosed Annotated Marked-up Drawings.

Finally, to place the drawings in sequential order, sheets 215-218 (Figs. 17V-17CC) of have been renumbered as sheets 75-78 (renumbered Figs. 17U-17BB), and sheet 219 (Fig. 18H) has been renumbered as sheet 92.

All of the foregoing amendments are incorporated in the Submission of Formal Drawings, enclosed herewith.

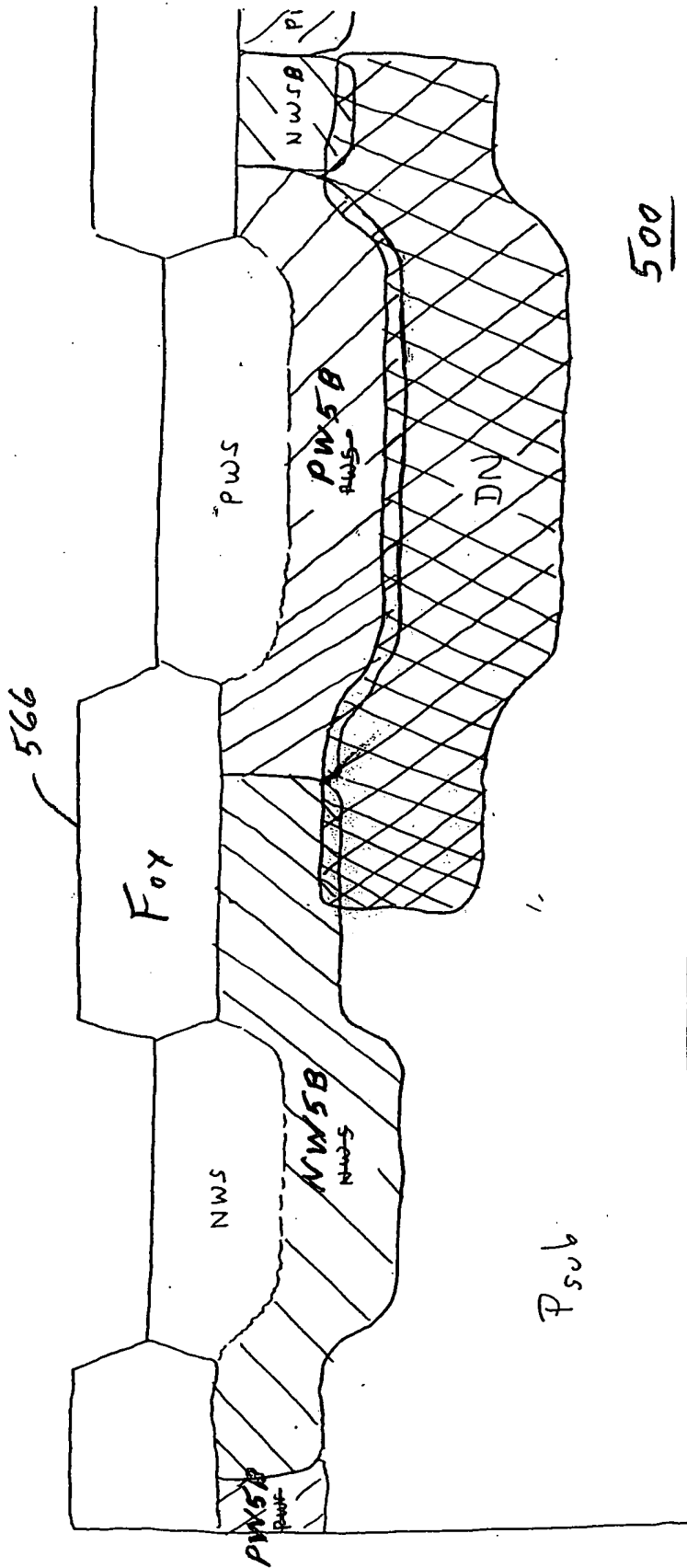
Attachment:           Annotated Sheets Showing Changes

Fig 14A



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Fig. 14 B



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Fig. 14 C

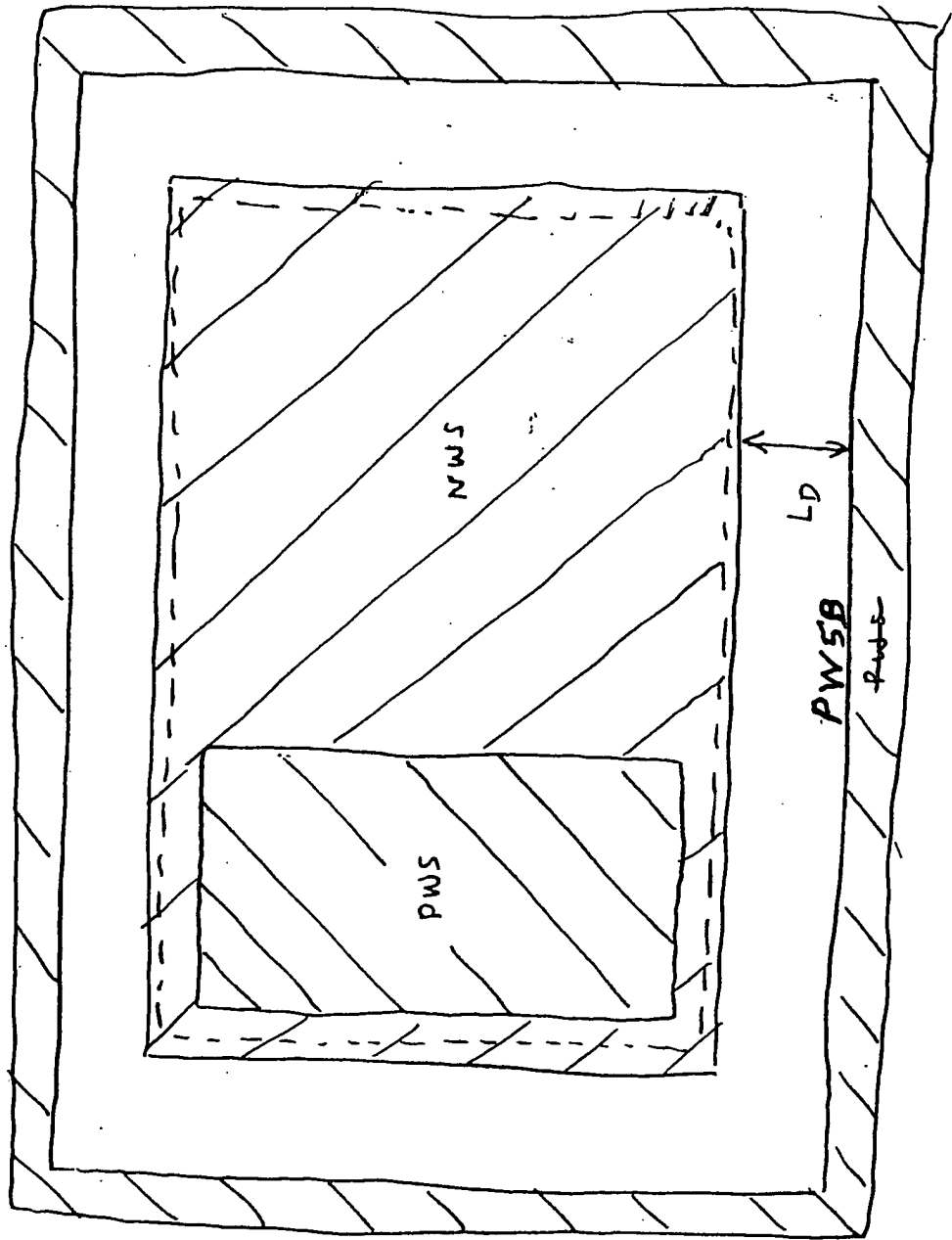


Fig 14D

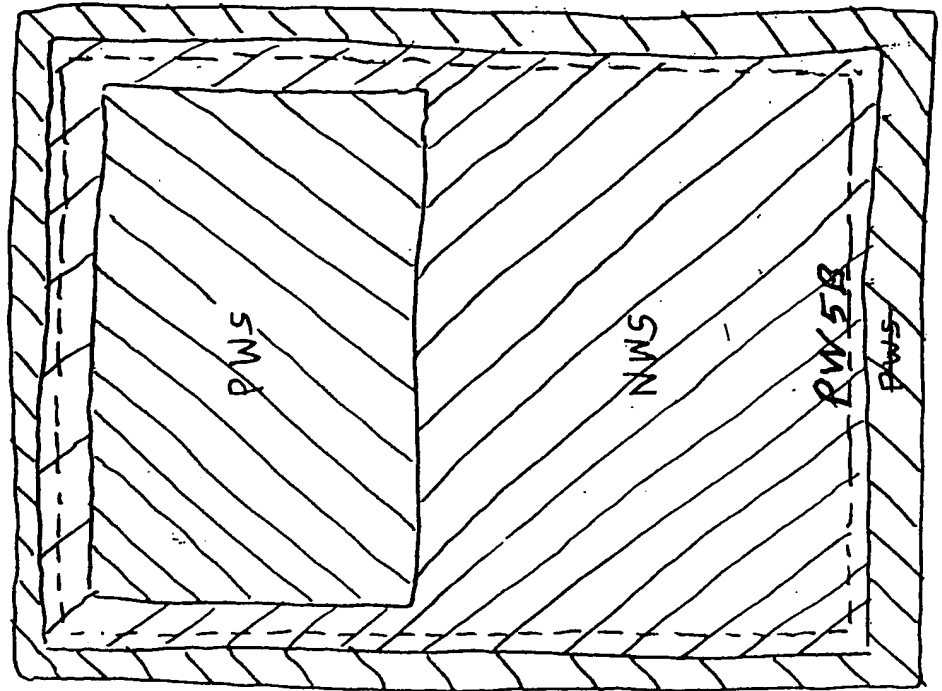
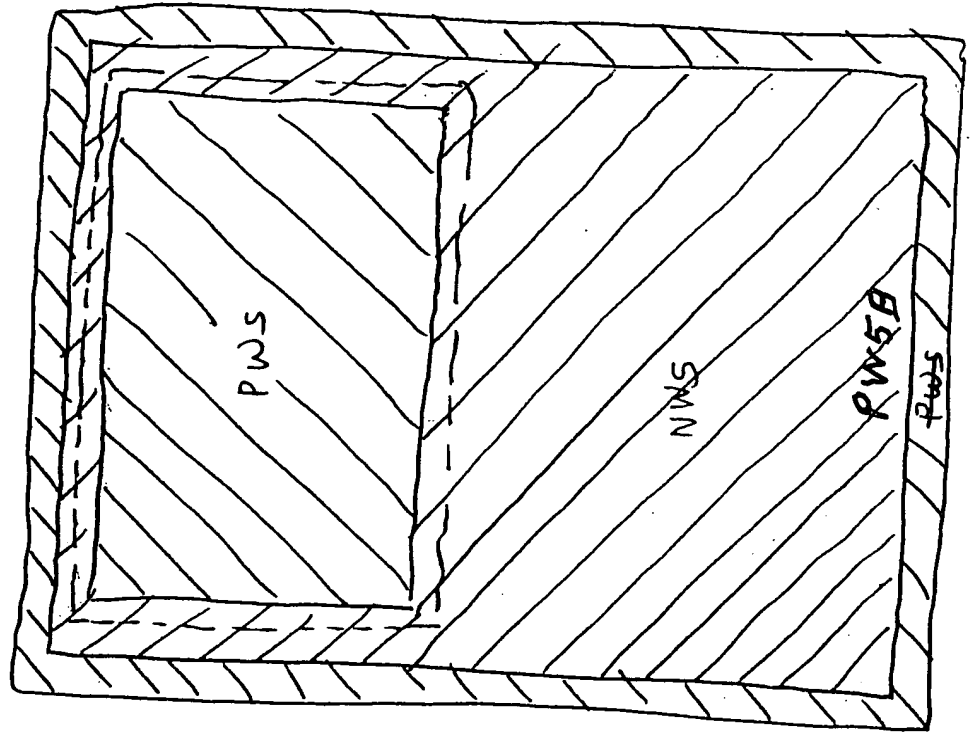


Fig. 14E



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Fig. 14H

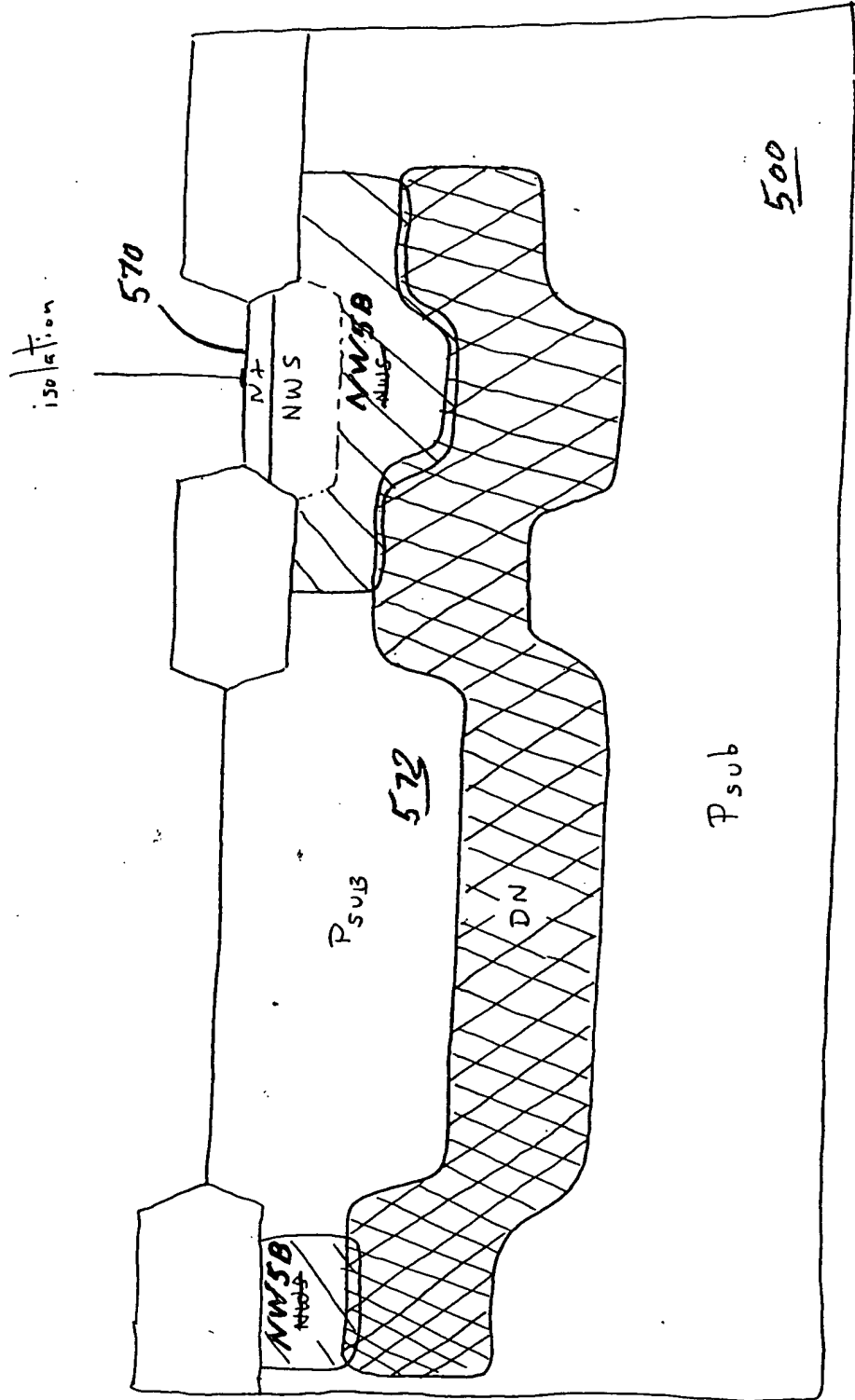




Fig. 14I.

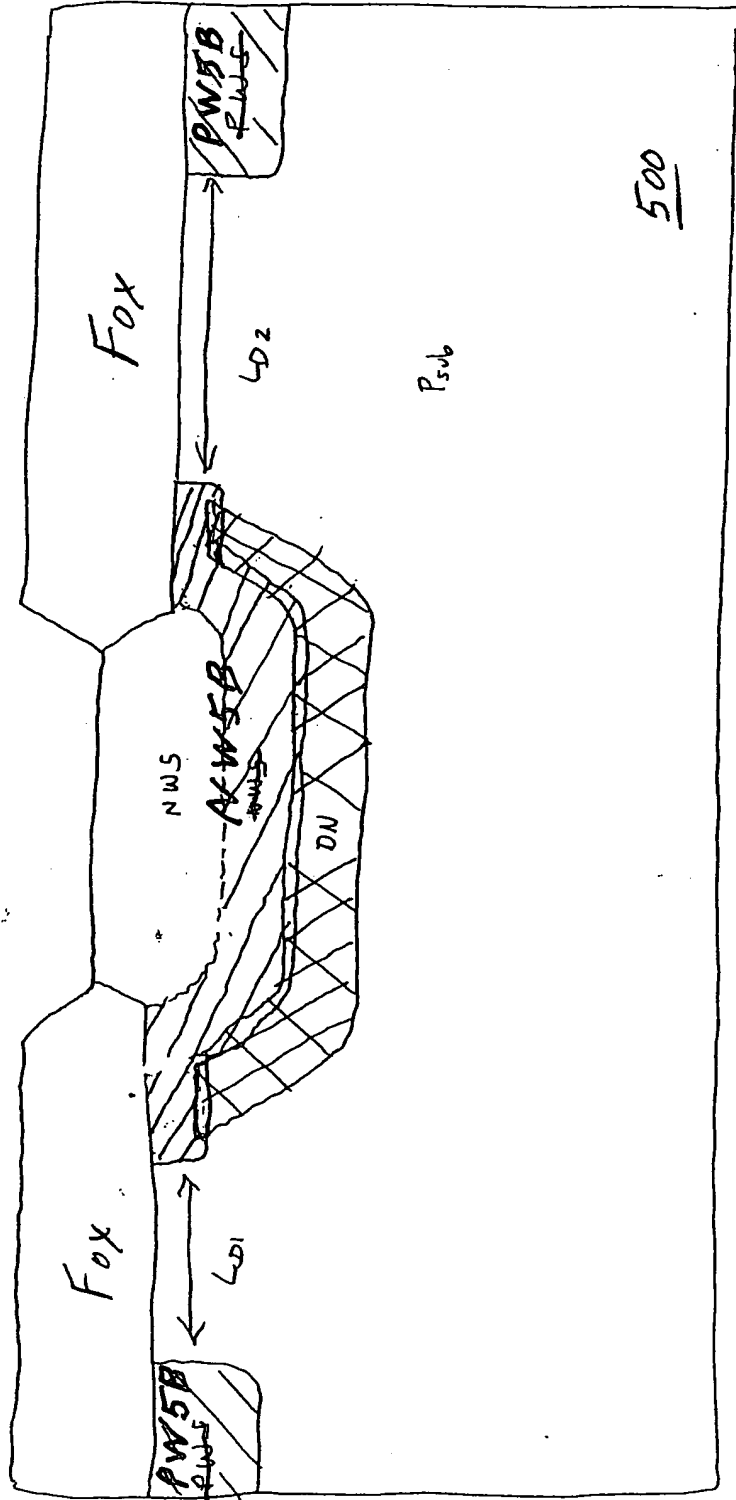


Fig. 14J

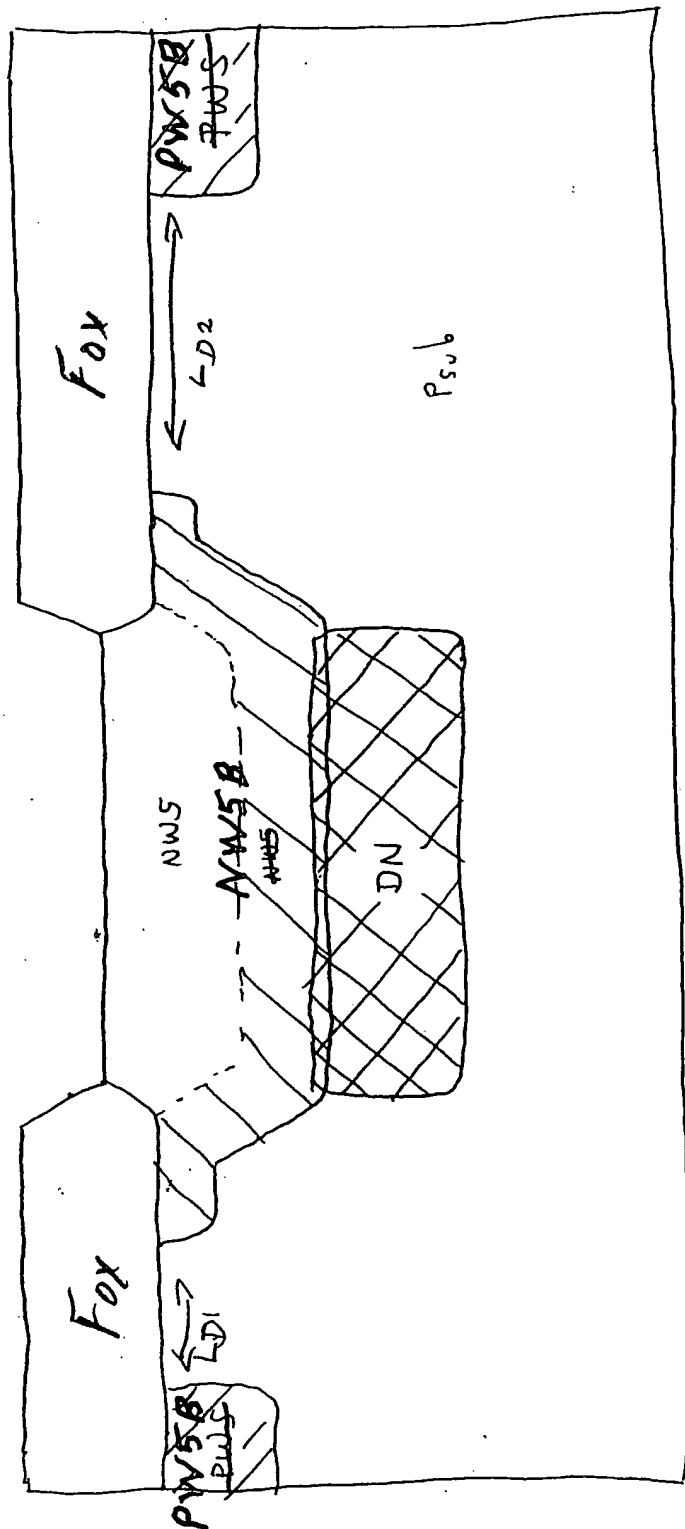


Fig. 14K

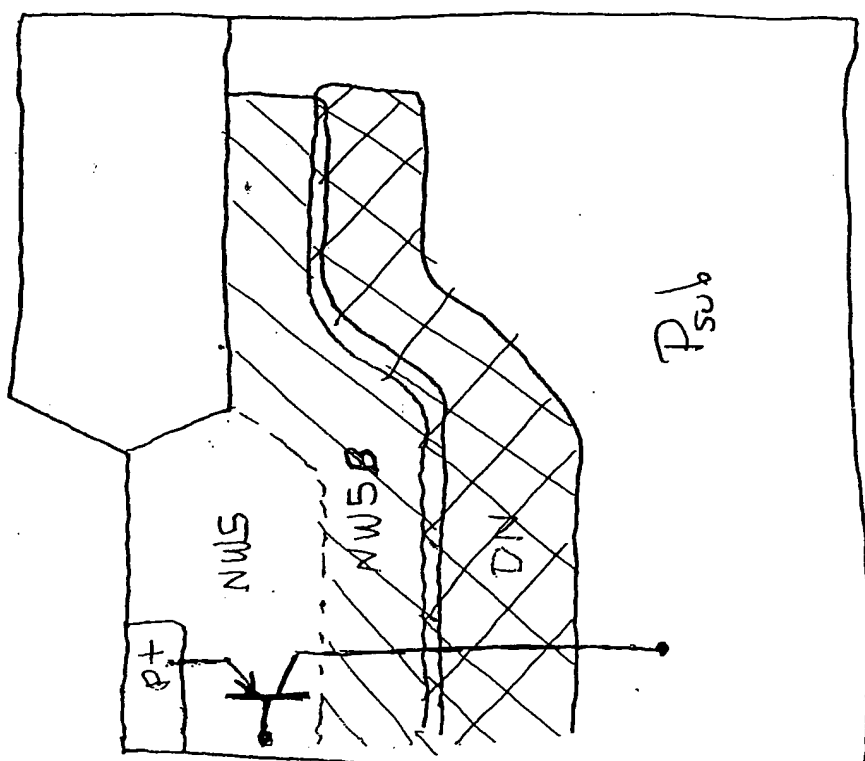


Fig. 14L

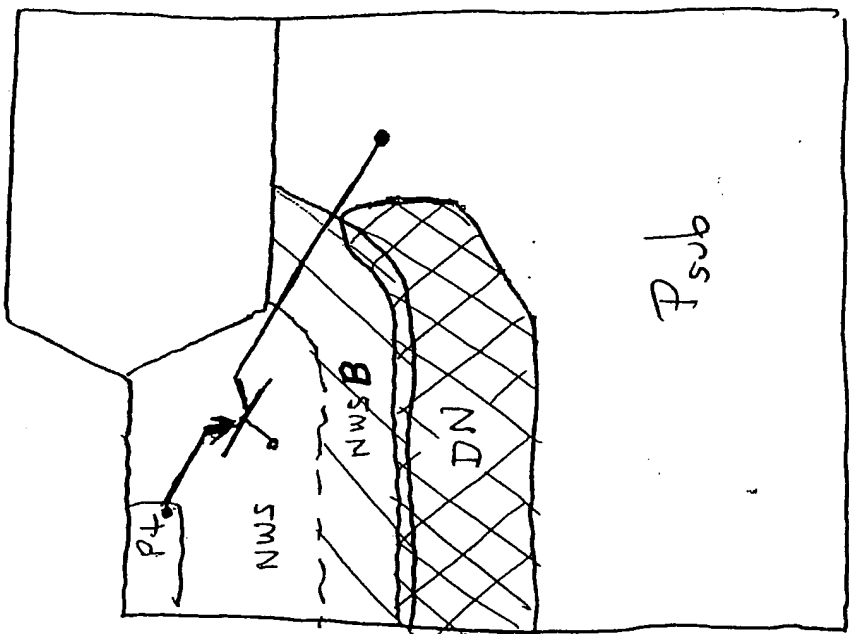


Fig. 14A

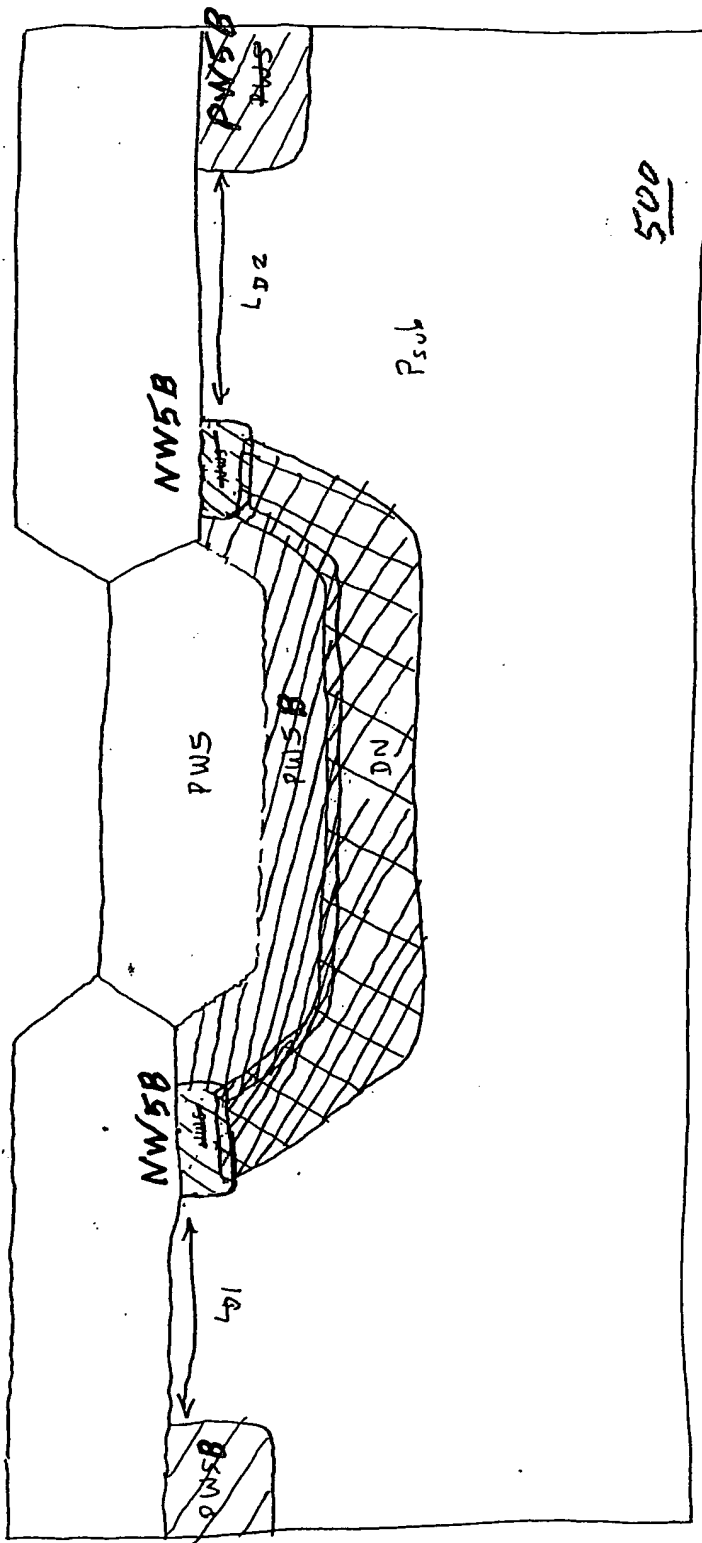


Fig. 14N

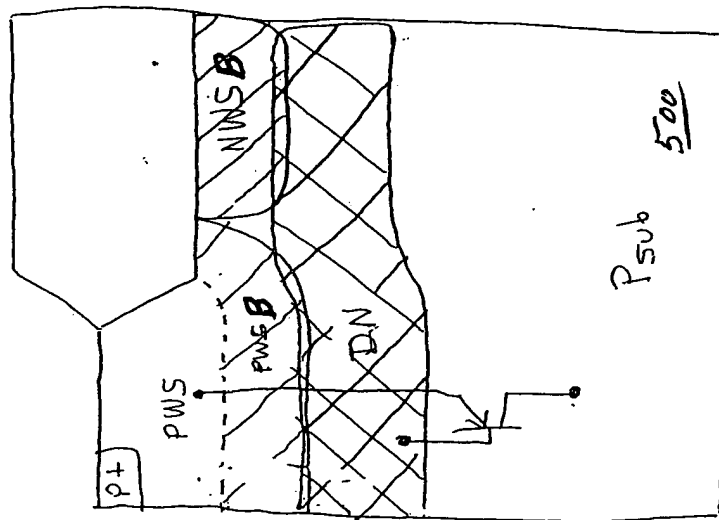


Fig. 14O

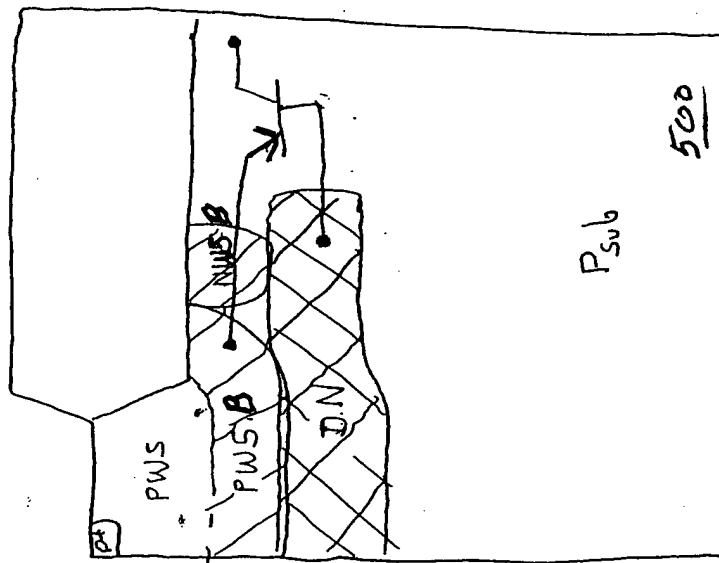


Fig. 14P

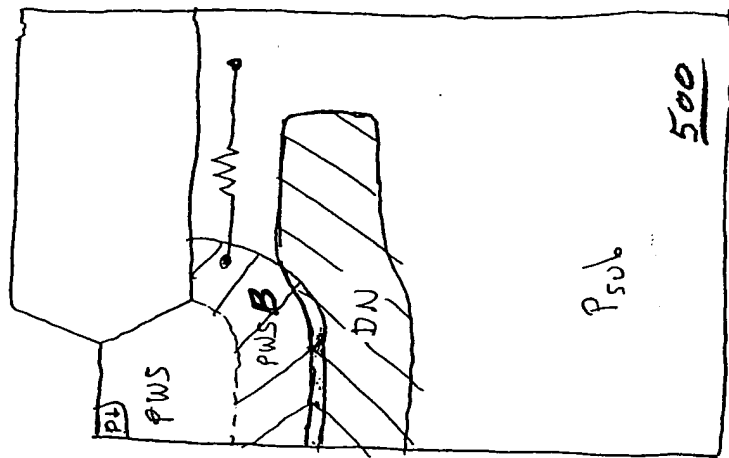


Fig. 15A

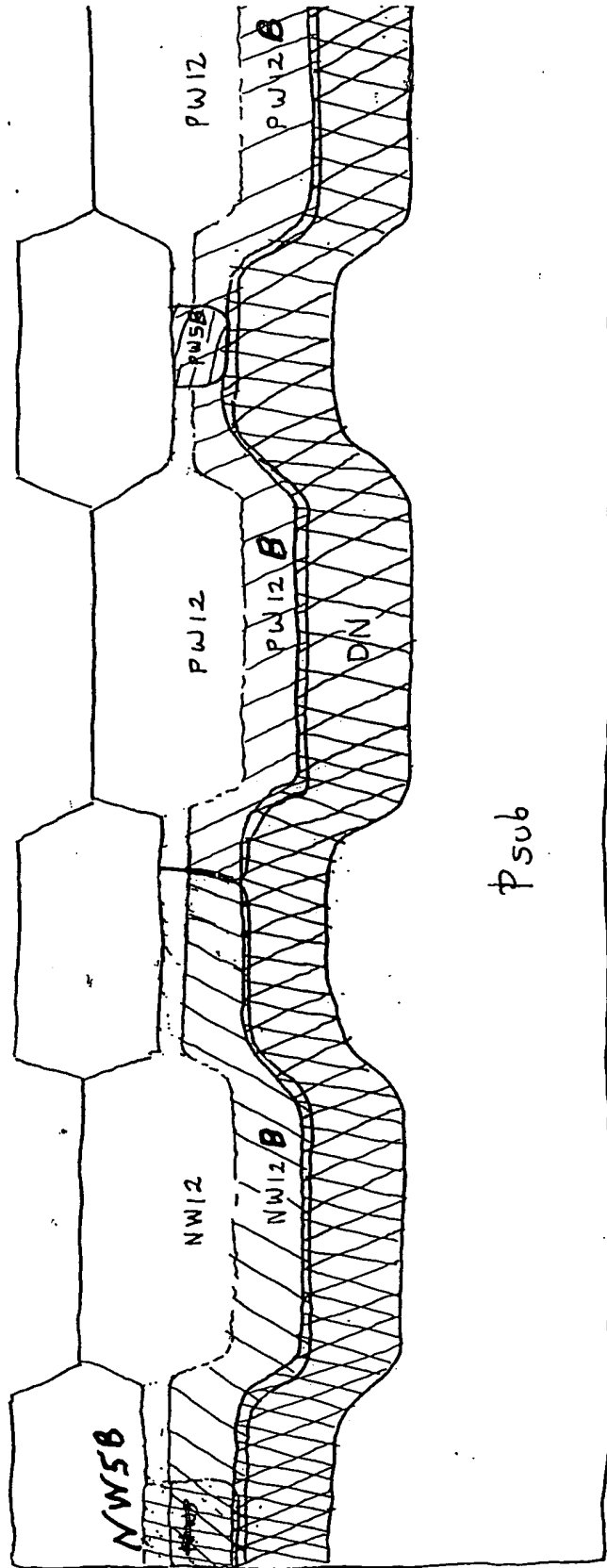




Fig. 16B

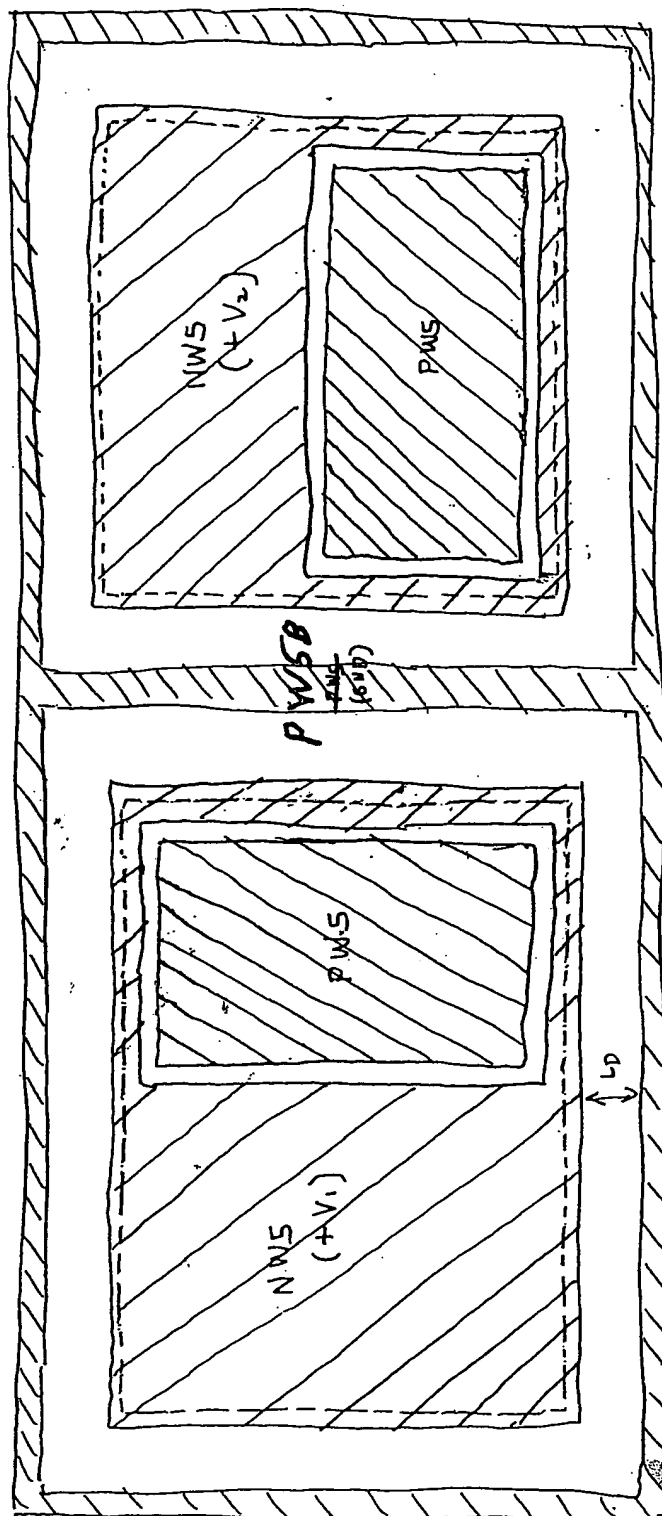
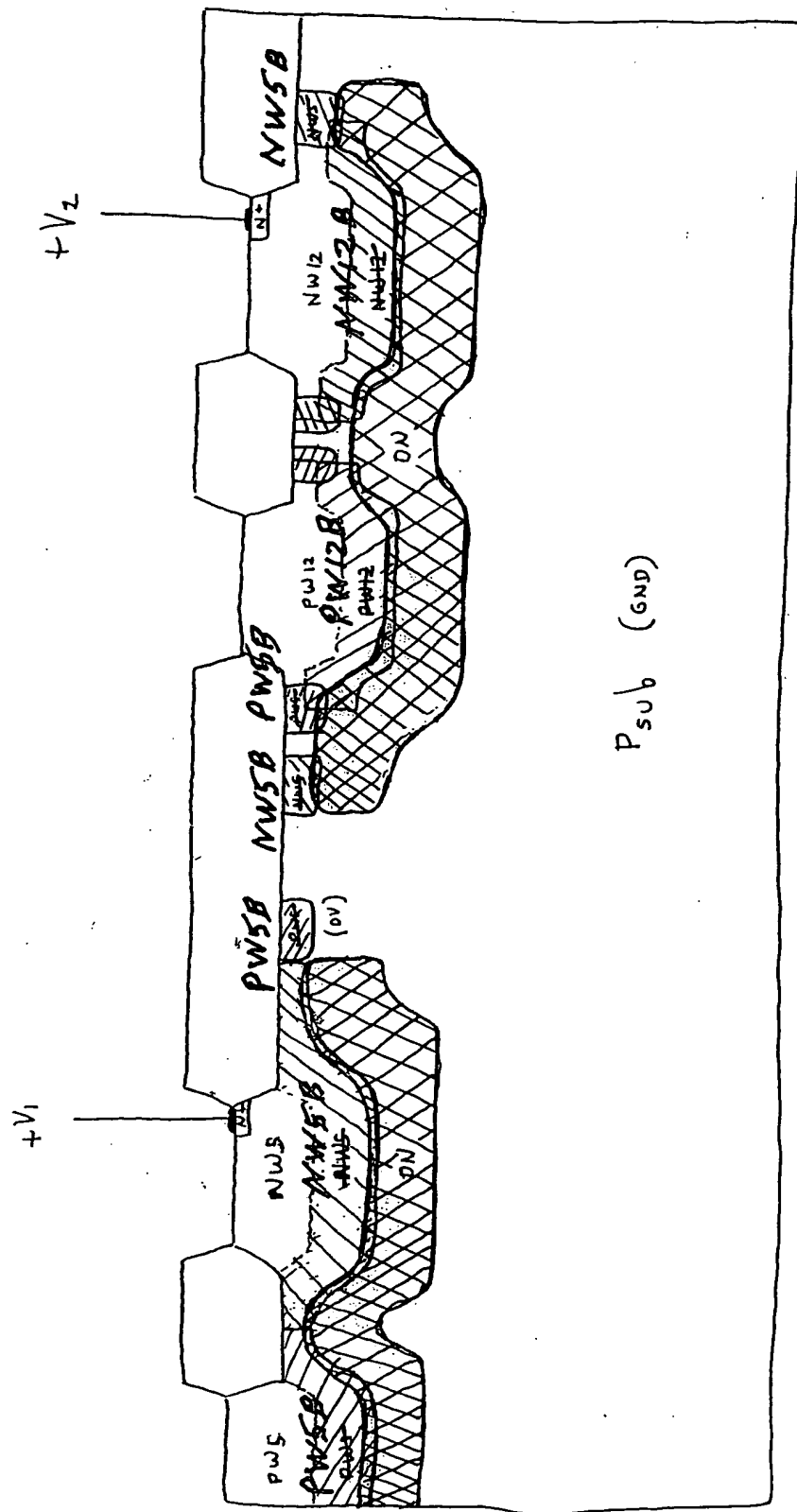




Fig. 16D



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Fig. 16F

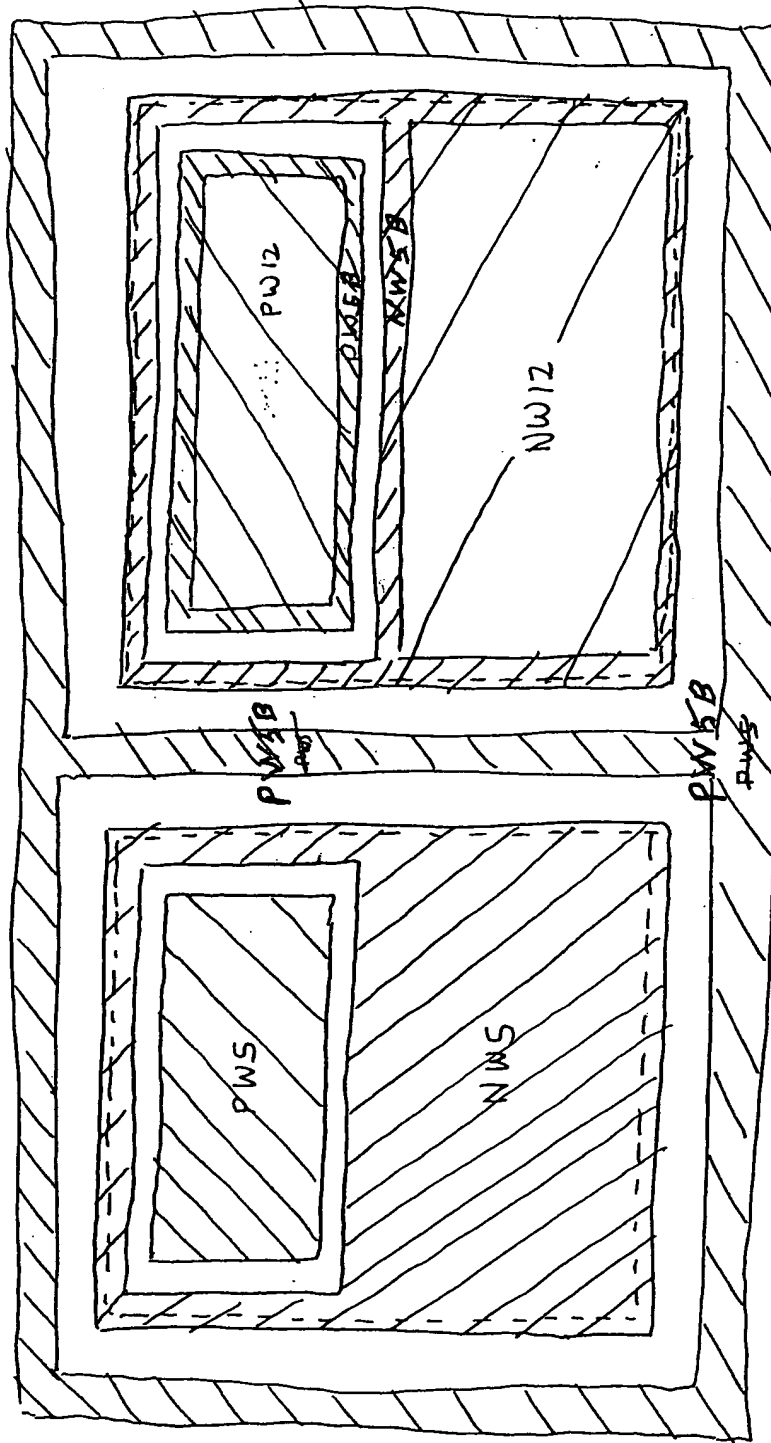


Fig. 17Q<sup>P</sup>

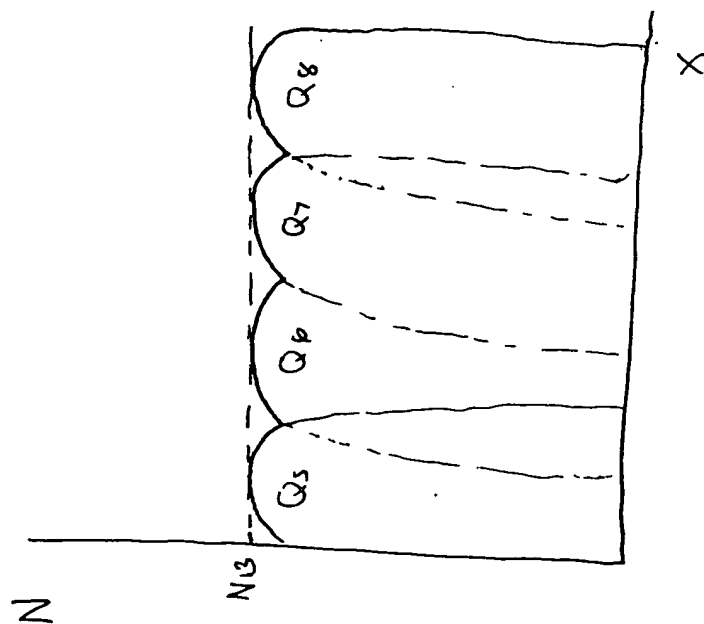
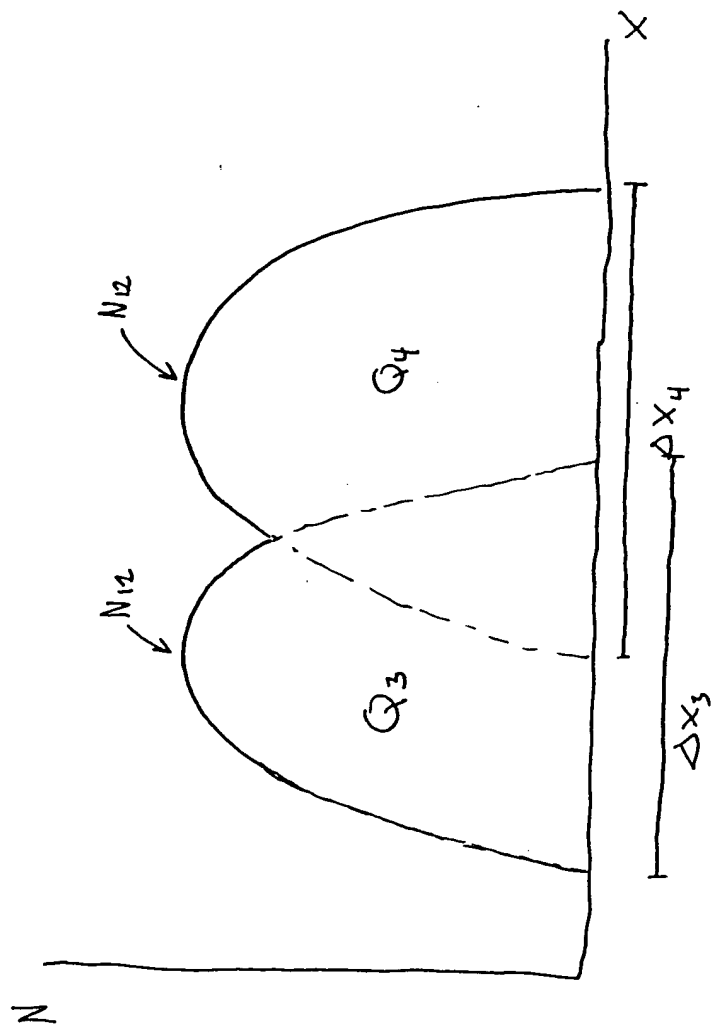
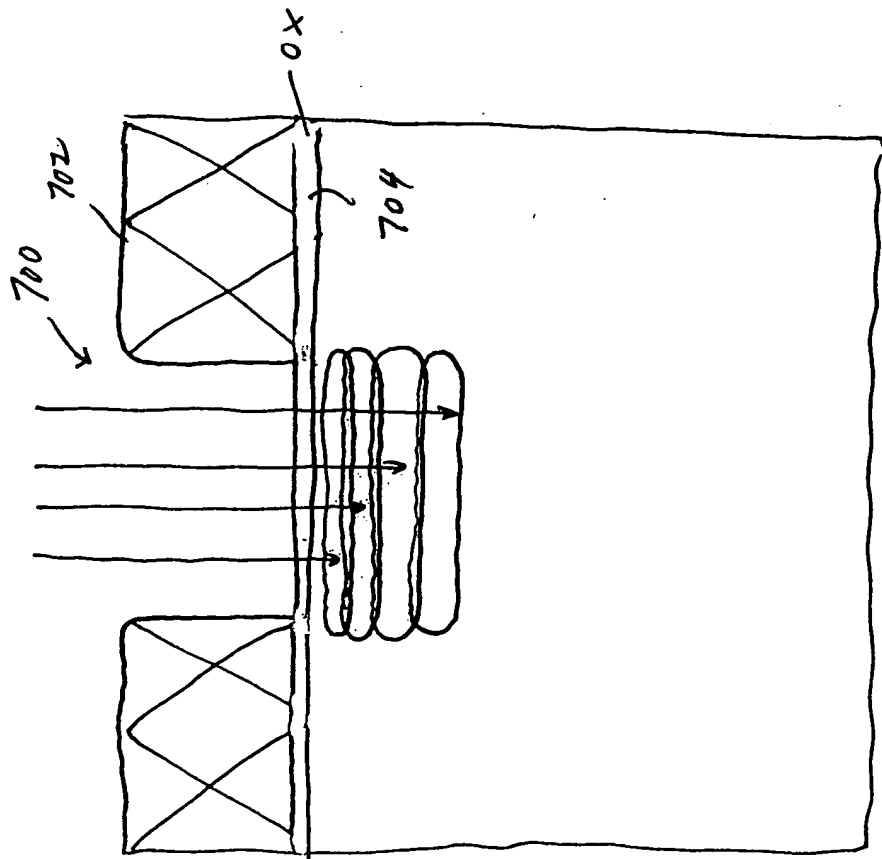


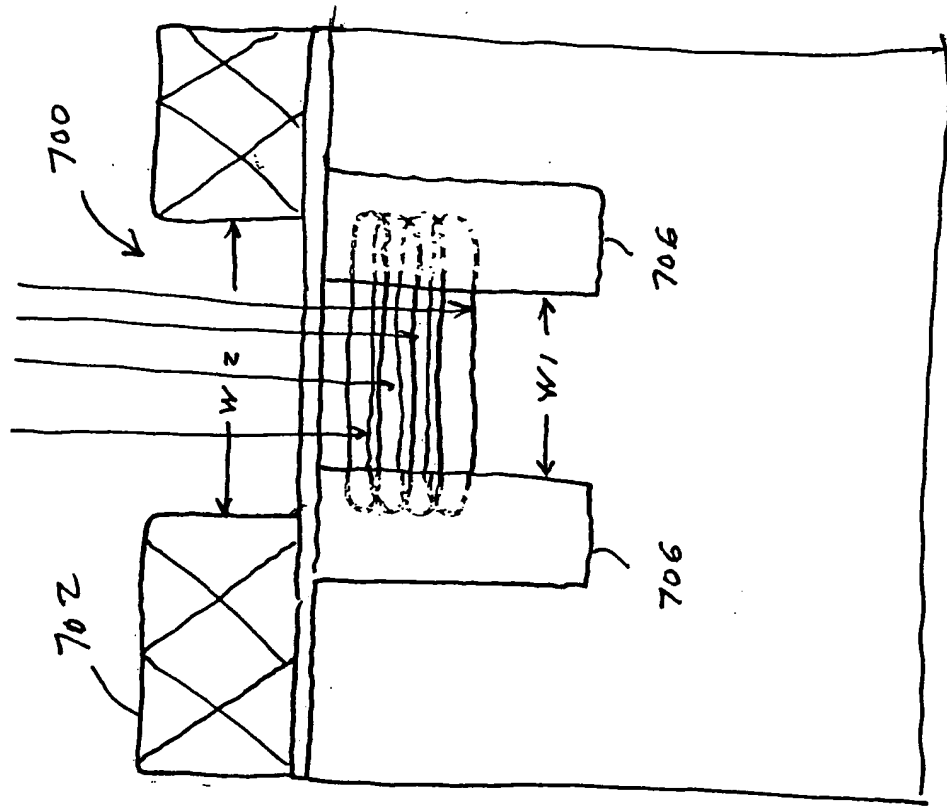
Fig. 17Q<sup>O</sup>



Q  
Fig. 17R



R  
Fig. 17S



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Fig. 17 <sup>S</sup>

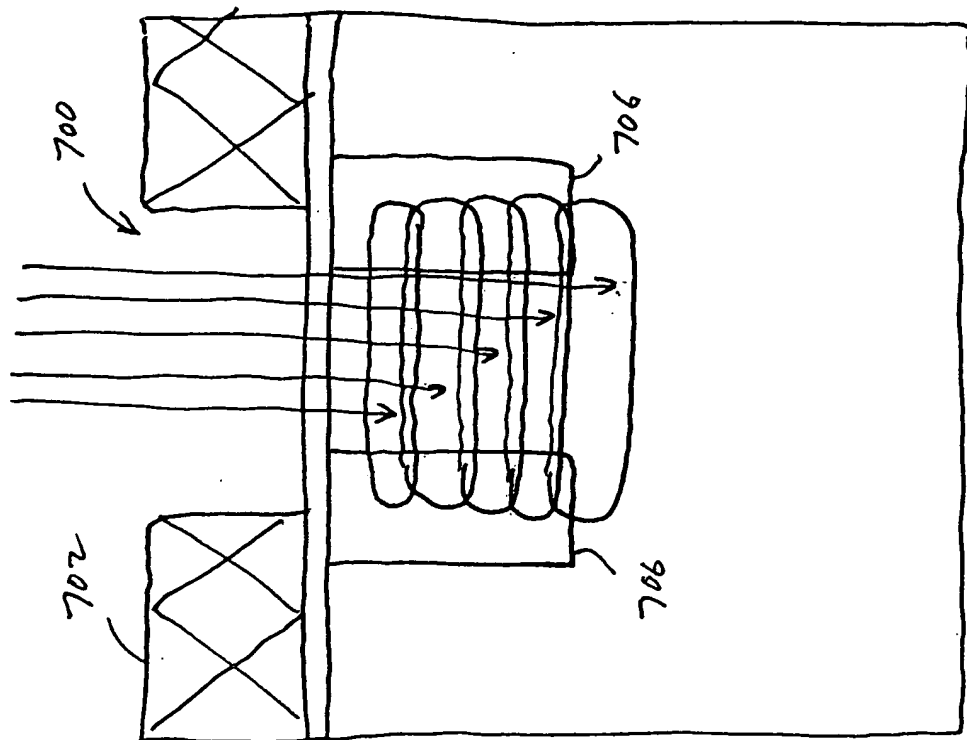
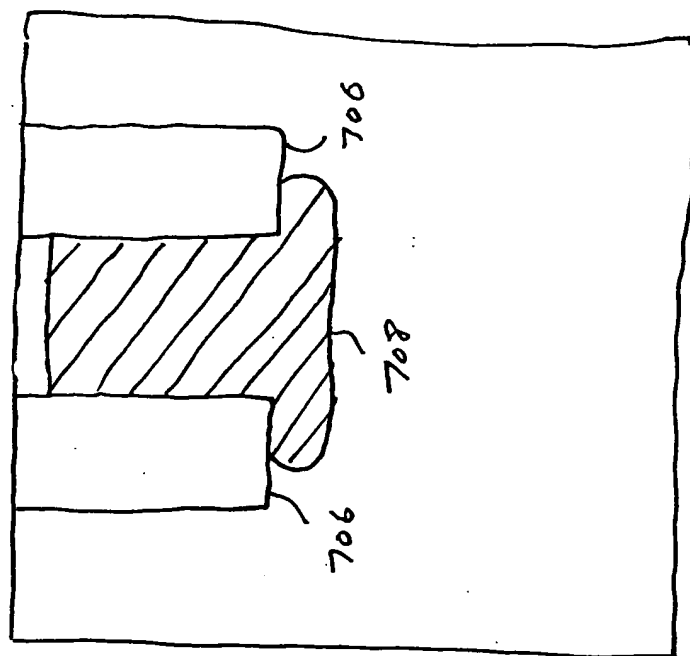


Fig. 17 <sup>T</sup>



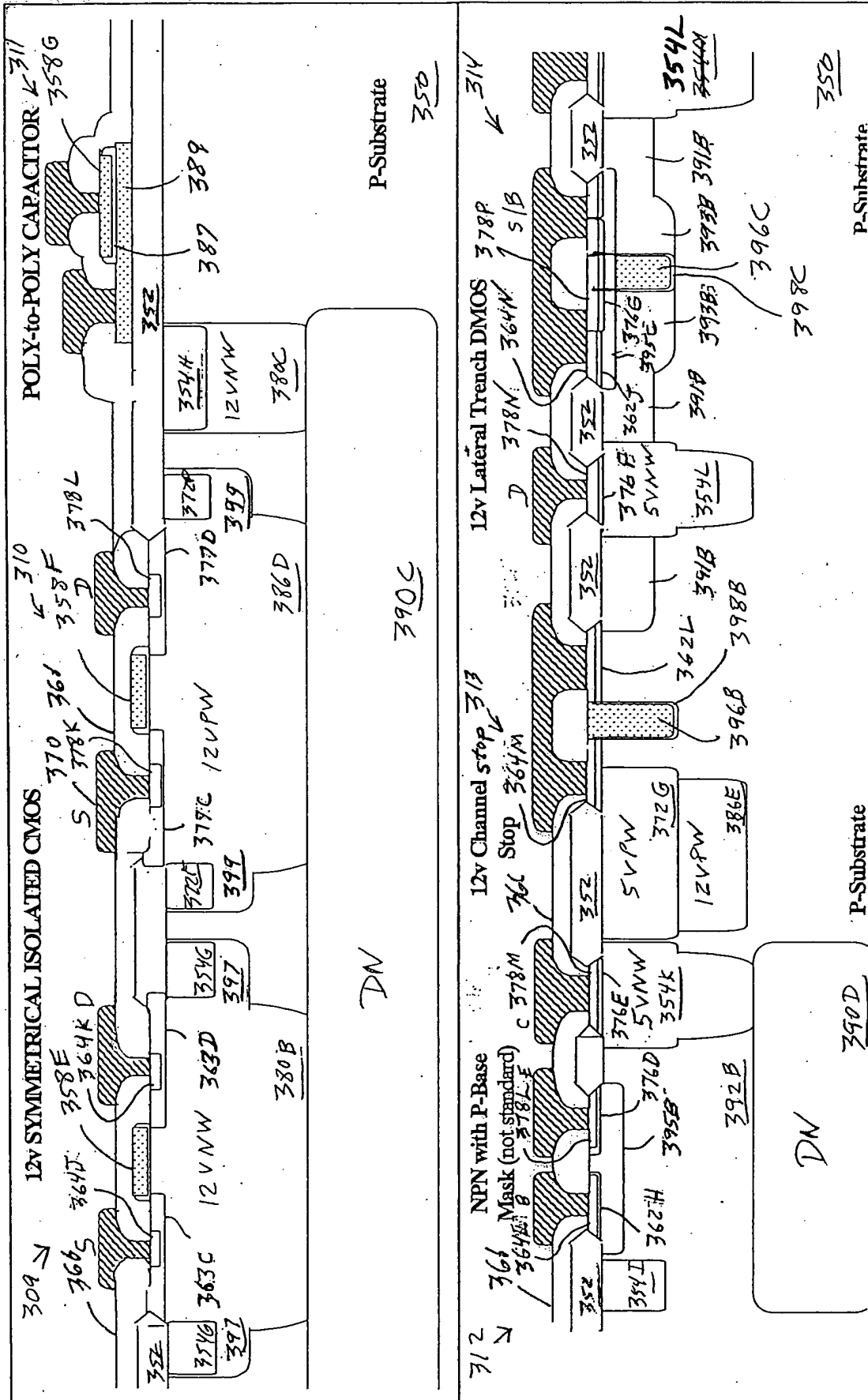


Fig. 18B

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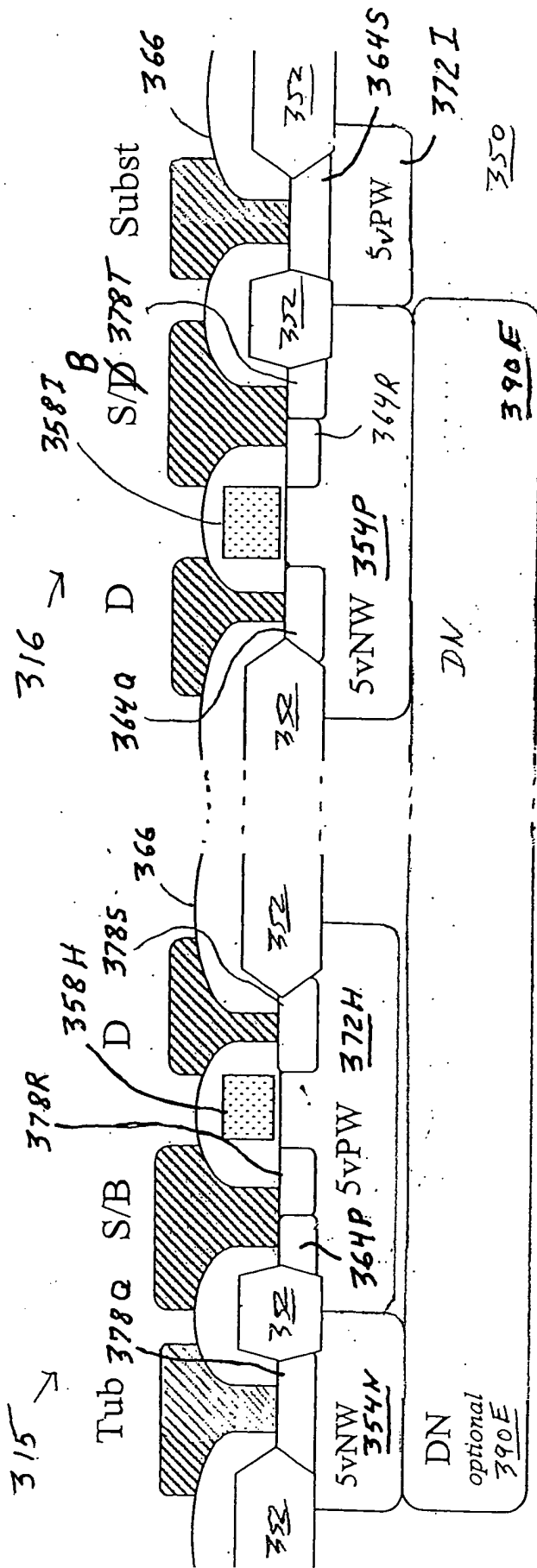
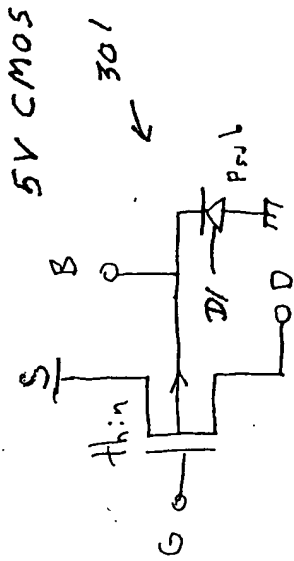


Fig. 18C



5V CMOS

301

12V CMOS

303

30V Trench LDMOS

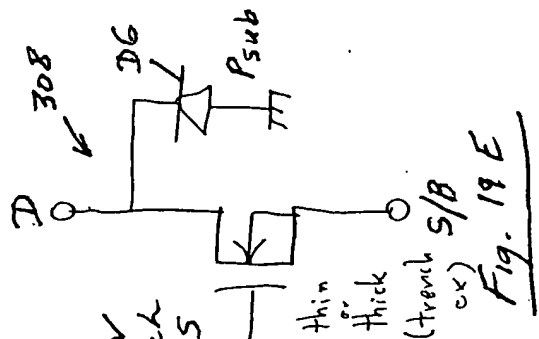


Fig. 19E

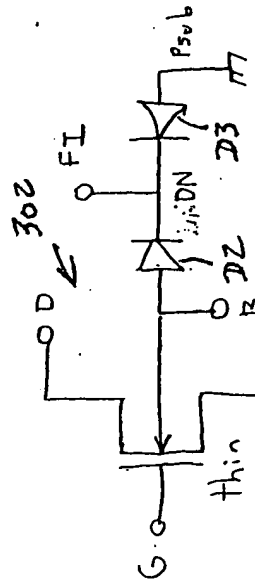


Fig. 19A

5V NPN

Fig. 19B

5V PNP

30V LDMOS

320 387

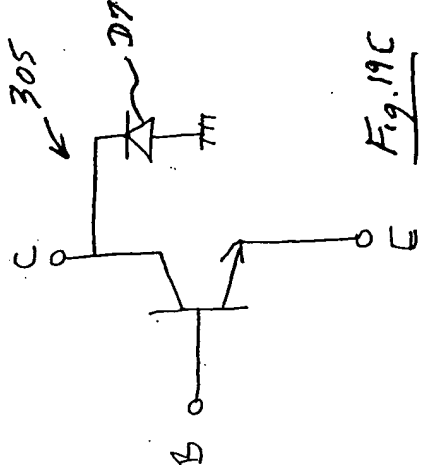


Fig. 19C

306

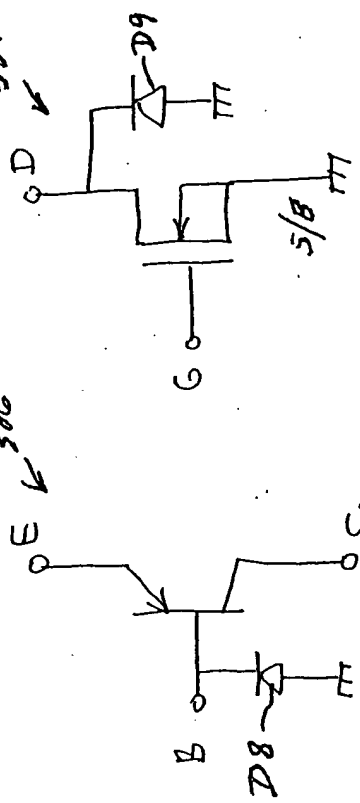


Fig. 19D

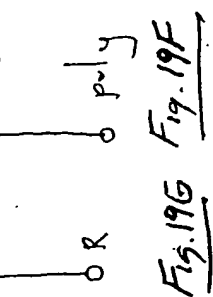


Fig. 19F

Fig. 19G

Fig. 19H

Fig. 19I

Fig. 19J

Fig. 19K

Fig. 19L

Fig. 19M

Fig. 19N

Fig. 19O

Fig. 19P

Fig. 19Q

Fig. 19R

Fig. 19S

Fig. 19T

Fig. 19U

Fig. 19V

Fig. 19W

Fig. 19X

Fig. 19Y

Fig. 19Z



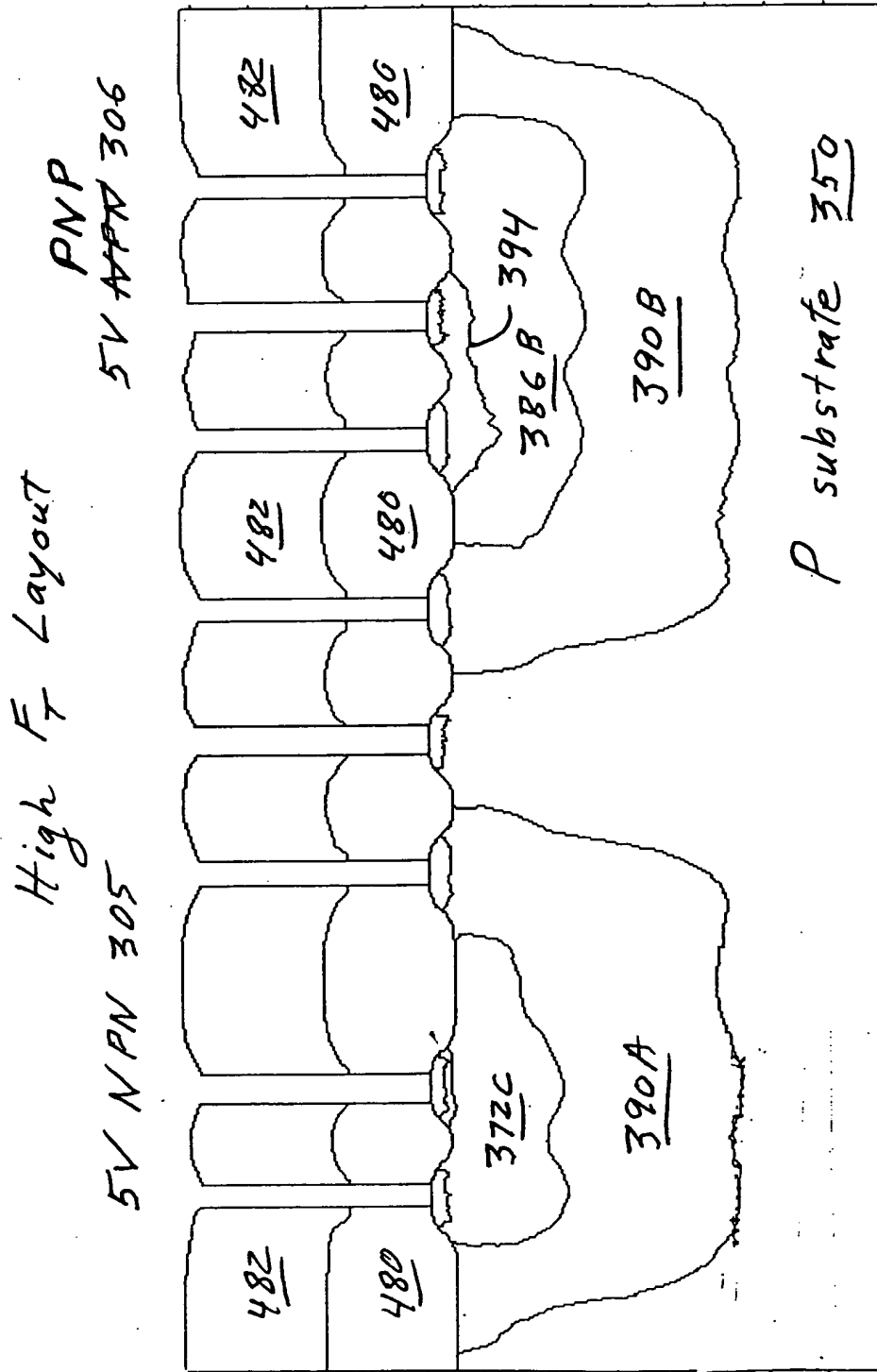
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## Interlayer Dielectric

Fig. 33D

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Interlayer Dielectric Deposition and Etch

Fig. 64B

Fig. 17<sup>U</sup>

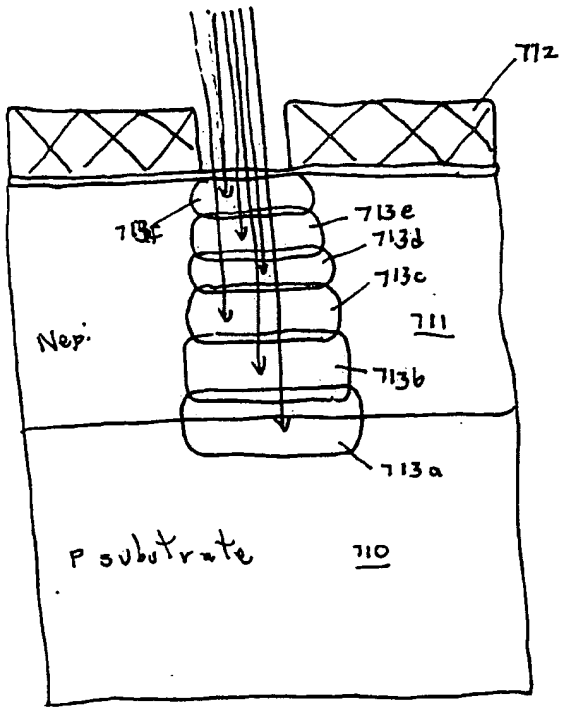


Fig. 17<sup>V</sup>

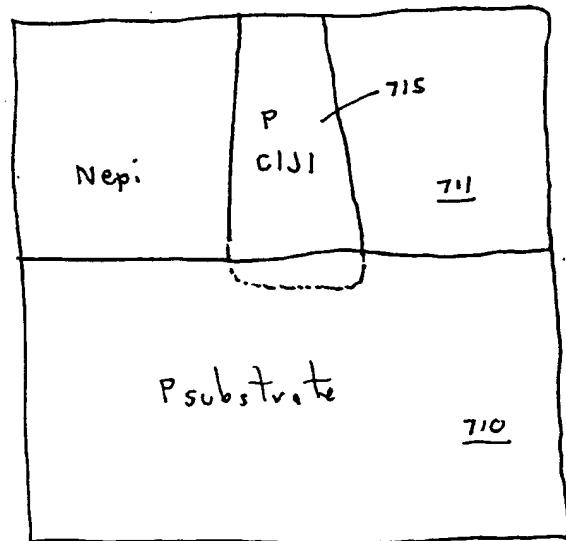


Fig. 17<sup>W</sup>~~X~~

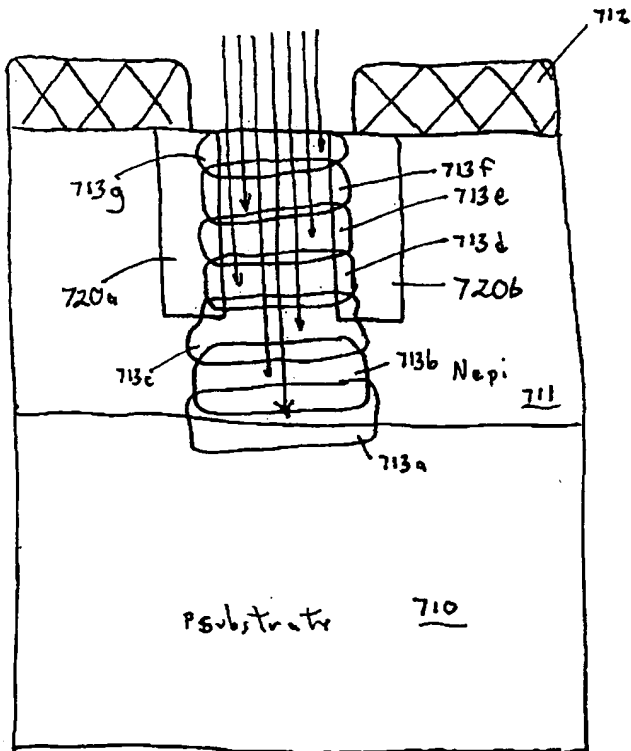
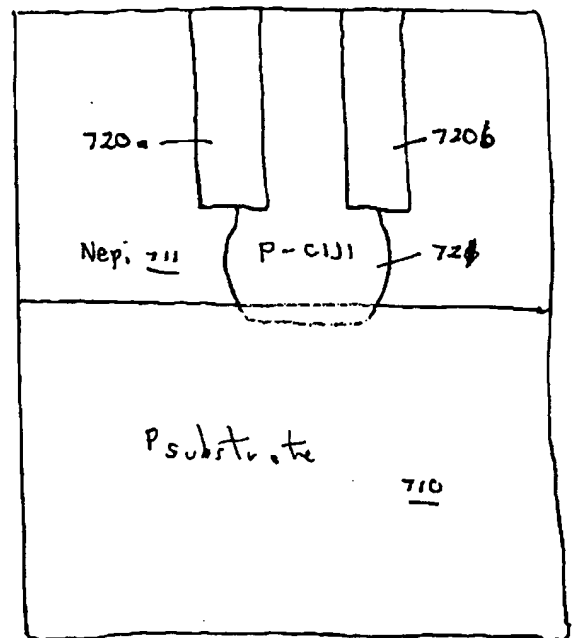
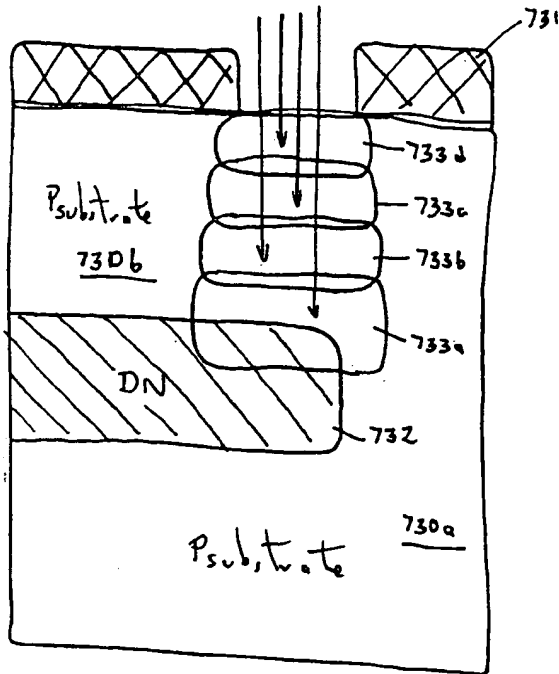


Fig. 17<sup>X</sup>~~X~~



Y  
Fig. 17



Z  
Fig. 17A

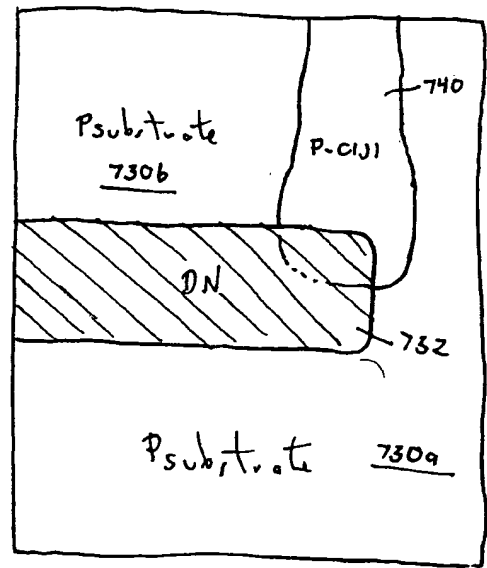
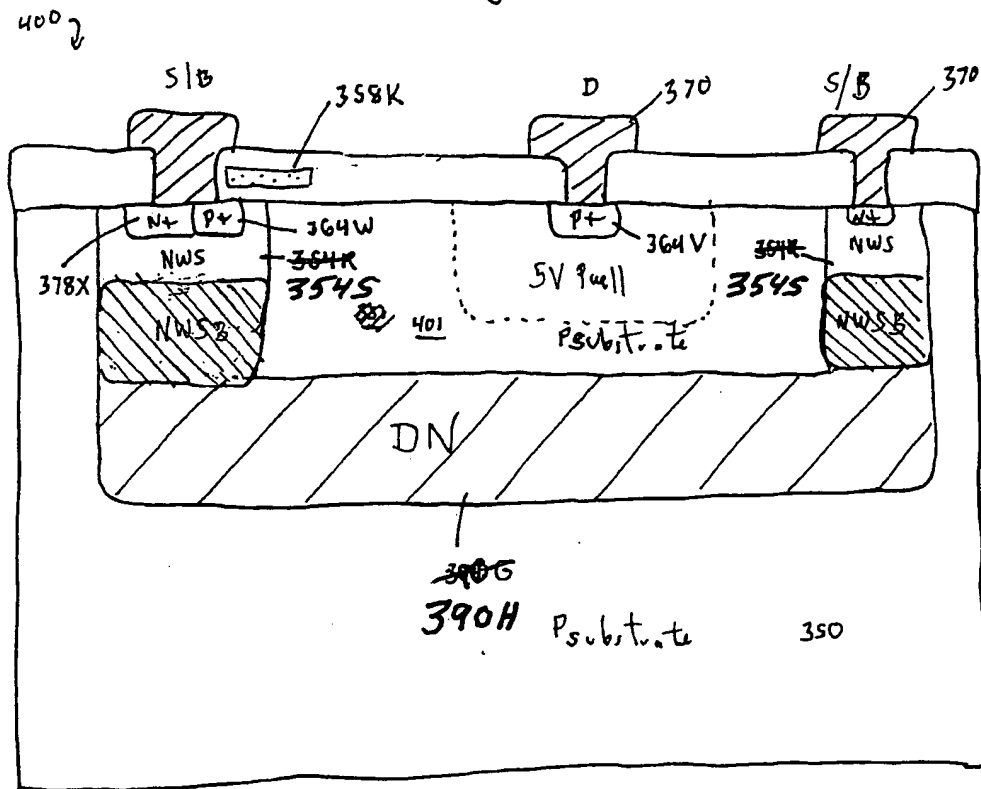




Fig. 18H



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